Haotian Lu

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Personal Page | Haotian Lu | TRIGGERONE | Haotian Lu

Education

- **University of California, Riverside** *09/2024 - 06/2029 (Expected)*
  Ph.D. in Electrical Engineering Riverside, CA
  - Advisor: Prof. Sheldon X.-D. Tan
  - Research Interests: ML-based VLSI Reliability Analysis, Efficient ML, Low-power Circuit Design
  - GPA: 4.0/4.0

- **Tianjin University** *09/2019 - 06/2023*
  B.E. in Integrated Circuits Design Tianjin, China
  - GPA: 3.84/4.0, Outstanding Graduate (Honors)

Publications

C=Conference, J=Journal

[C2] **The Unlikely Hero: Nonideality in Analog Photonic Neural Networks as Built-in Defender Against Adversarial Attacks**.
Haotian Lu, Ziang Yin, Partho Bhoumik, Sanmitra Banerjee, Krishnendu Chakrabarty, Jiaqi Gu.
ACM/IEEE Asian and South Pacific Design Automation Conference (ASP-DAC), Tokyo, Japan, Jan. 20-23, 2025.

[C1] **Energy-efficient NTT Design with One-bank SRAM and 2-d PE Array**.
Jianan Mu, Huajie Tan, Jiawen Wu, **Haotian Lu**, Chip-Hong Chang, Shuai Chen, Shengwen Liang, Jing Ye, Huawei Li, Xiaowei Li.
IEEE Design, Automation & Test in Europe Conference & Exhibition (DATE), Antwerp, Belgium, Apr. 17-19, 2023.

[J2] **DOCTOR: Dynamic On-Chip Temporal Variation Remediation Toward Self-Corrected Photonic Tensor Accelerators**
Haotian Lu, Sanmitra Banerjee and Jiaqi Gu.
IEEE Journal of Lightwave Technology (JLT), Jun. 2024.

[J1] **Investigating on sensing mechanism of MoS2-FET biosensors in response to proteins**.
Ziheng Ji, Junqing Wei, Fengting Luo, Zihao Liu, **Haotian Lu**, Ruibing Chen, Yong Wang, Guoxuan Qin.
Nanotechnology, Aug. 2023.

Experience

- **VSCLAB @ Univeristy of California, Riverside[]** *09/2024-Present*
  Graduate Student Researcher, Advisor: Prof. Sheldon X. -D. Tan Riverside, CA
  - Focusing on VLSI Reliability and Optimization against Electromigration.

- **ScopeX Group @ Arizona State University []** *06/2023 - 07/2024*
  Research Intern, Advisor: Prof. Jiaqi Gu Remote
  - Proposed a novel modeling method for real-world noise of optical devices and Photonic Tensor Core, developed a novel methodology for on-chip inference accuracy recovery against temporal variations [J2].
  - Explored inherit non-idealities of Photonic IC and designed low-cost defense framework against Adversarial Bit-flip Attack [C2].

- **State Key Laboratory of Processors, ICT, Chinese Academy of Sciences []** *04/2022 - 06/2023*
  Visiting Research Assistant, Advisor: Dr. Jianan Mu, Prof. Jing Ye Haidian District, Beijing, China
  - Participated in the design of low-power hardware implementation of NTT algorithm and produced its experimental results such as power consumption, timing and area using Synopsys DC [C1].
  - Focused on hardware acceleration of FHE schemes (especially CKKS) and participated in building basic components of several important operations using Spinal HDL.
  - Involved in paper writing and assisted engineers in front-end verification.

Skills

- Software: Python (Pytorch), C/C++, Matlab.
- Hardware Design: Verilog, SystemVerilog, Spinal HDL.
- EDA Tools: Cadence Virtuoso, Synopsys Design Compiler.